

Wet Processing for Post-epi & Pre-furnace Cleans in Silicon Carbide Power MOSFET Fabrication

J. J. McMahon^a, M. Jahanbani^b, S. Arthur^a, D. Lilienfeld^a, P. Gipp^a, T. Gorczyca^a, J. Formica^c, L. Shen^c, M. Yamagami^d, B. Hillard^e and J. Byrnes^e

^a GE Global Research Center, Niskayuna, NY, 12309, USA

^b SUNY Polytechnic Institute, Albany, NY, 12203, USA

^c Rigaku Americas Corporation, The Woodlands, TX, 77381, USA

^d Rigaku Corporation, Osaka, 569-1146, Japan

^e Semilab USA LLC, North Billerica, MA, 09654, USA

Silicon carbide (SiC) device fabrication technology shares many similarities with Si manufacturing, but identifying whether material differences affect cleaning capability is of interest for this growing field. Material parameter differences include diffusion coefficients, surface energy, and chemical bond strength, all of which can play a role in cleaning critical surfaces. This work compares trace surface contamination levels (as measured by TXRF) after 100 mm or 150 mm 4H SiC wafers underwent mercury-probe capacitance voltage (MCV) mapping, to levels after subsequent cleans. Trace levels of metals such as Hg, Fe, and Ni were controllably added during MCV, and it was shown that a variety of cleaning approaches can return the SiC surface to sub- 5×10^{10} atoms/cm² levels of cleanliness. Where these cleans fit into an integrated device process flow and comparison of cost are discussed.

Introduction: SiC MOSFETs Entering Volume Production

Silicon carbide (SiC) power devices provide improved switching efficiency and are well-suited for high-temperature and medium- to high-voltage applications (1, 2). As such, they are expected to spur growth for applications > 1000 V over the next decade as they enable significant reduction in emissions (3). The Power Electronics Manufacturing Consortium at SUNY Polytechnic is positioned to take advantage of this growth, as it ramps up moderate volume for 1200 V power metal-oxide-semiconductor field-effect transistors (MOSFETs) using 150 mm SiC wafers (4, 5). This ramp provides an opportunity to delineate development issues that are an impediment to volume manufacture of SiC MOSFETs, including risks to cost, throughput, yield, and reliability. If any of these parameters are affected by material differences (between Si and SiC), then identifying those issues and building a roadmap for improvements to be inserted into volume manufacturing will be required.

The chemically inert nature of SiC presents unique opportunities and challenges with regard to cleaning and surface preparation during fabrication of power MOSFETs. Previous investigations (6-8) have proposed alternate chemistries to address such challenges, but here we present results for cleans post-epi test, also known as initial wafer clean (IWC), and pre-furnace clean based on concentrated chemistries developed for Si

and transferred to SiC, and we discuss cleaning capability and cost tradeoffs for dilute chemistries as SiC technology ramps from pilot to volume production.

Although the diffusion of materials in single-crystal SiC is much slower than that found in Si for similar temperatures (9), SiC thermal processing generally occurs at much higher temperatures and therefore metal contamination must be minimized to maintain process control and reliability. Furthermore, minimizing metallic impurities in oxides grown on SiC is critical because iron, nickel, and other metallics are understood to degrade intrinsic lifetime of gate oxides (10, 11). Thus, these metals are monitored for SiC processing at levels comparable to appropriate Si technology nodes; in this case, the ITRS FEP specification used for the 180nm node is expected to be adequate (12). TXRF is an effective diagnostic tool used in controlling these contaminants, so it is employed by measuring Si and SiC monitor wafers run alongside device lots at pre-furnace cleans and high-temperature furnace processing steps. Additionally, 1200 V SiC MOSFETs are fabricated on epitaxially grown N- layers; those layers are typically characterized with mercury (Hg) probe capacitance-voltage (MCV), leaving trace levels of Hg on the SiC wafer surface (13). Thus, in addition to the typical metal concerns, Hg must be removed before wafers proceed into the fabrication process flow.

Mercury-probe CV (MCV), TXRF, and Cleaning Experiments

In order to controllably introduce contaminants to the SiC surface and test cleaning capabilities, 100 mm and 150 mm ultra-low micropipe density epi-ready SiC wafers were Hg probed in a Semilab MCV-530 tester, trace metal contaminants were measured using TXRF, wafers were cleaned in a variety of different cleaning chemistries, and post-cleaned wafers were again analyzed for trace impurities. The MCV measurement was performed using several multi-measurement patterns such as radius scan, wafer mapping, and measuring in the same location multiple times, which enabled the first TXRF measurement to compare uncontaminated areas vs. contaminated areas, and the post-cleaned TXRF to compare to the pre-cleaned state.

MCV measurements begin with Hg withdrawn ~0.5 mm to 2 mm within the 1.7 mm glass capillary, then the capillary is lowered until it is in contact with the surface of the wafer, pressure of ~5 kPa forces the Hg into contact with the SiC surface and the measurement is made. Pressure is released and the Hg is withdrawn back into the capillary, and the process is repeated. The probe descent time is about 1 sec and the measurement time is about 2 sec. The first set of MCV processing was performed on two 100 mm SiC wafers and was run using a 44-point map with many locations being measured multiple times in order to establish baseline characteristics regarding variability. The second set of MCV processing experiments were performed on 150 mm wafers. The left panel in Figure 1 illustrates a radial scan of 10 MCV points, each approximately 1.7 mm in diameter. The intent of this measurement pattern was to allow uncontaminated areas to be compared to contaminated areas, as the larger spots represent 10 mm diameter TXRF measurement locations. These wafers received additional repeatability measurements near the wafer center, one wafer was repeated 5x, and another was repeated 2x on the front and 3x on the back (wafer placed face-down on the chuck). A full 55-point MCV map was also performed on two 150 mm wafers.

After MCV, wafers were sent out for trace contamination analysis. Initial TXRF was performed within 3-5 days of Hg probing on one of two tools: 100 mm SiC wafers were analyzed in a legacy Technos TREX instrument and 150 mm SiC wafers were

analyzed in a Rigaku model 3760 instrument with advanced capabilities (such as sweeping mode and zero-edge exclusion). The 100 mm wafers were analyzed for Hg only, so utilized a molybdenum anode for excitation and utilized 15 mm edge exclusion. 150 mm wafers were analyzed for both heavy elements and transition metals, so used the W-L β line and the W-H.E. analysis modes. Measurement patterns for the 150 mm analyses are also presented in Figure 1: the left panel shows a 5-point map used for measurements that require longer times to reach the sensitivities required for this study (such as Hg), and the right panel illustrates a 165-point map for measurements with high sensitivity, such as Fe and Ni. Analyzing SiC wafers for trace contaminants presents a variety of challenges, which are discussed in detail elsewhere (14).

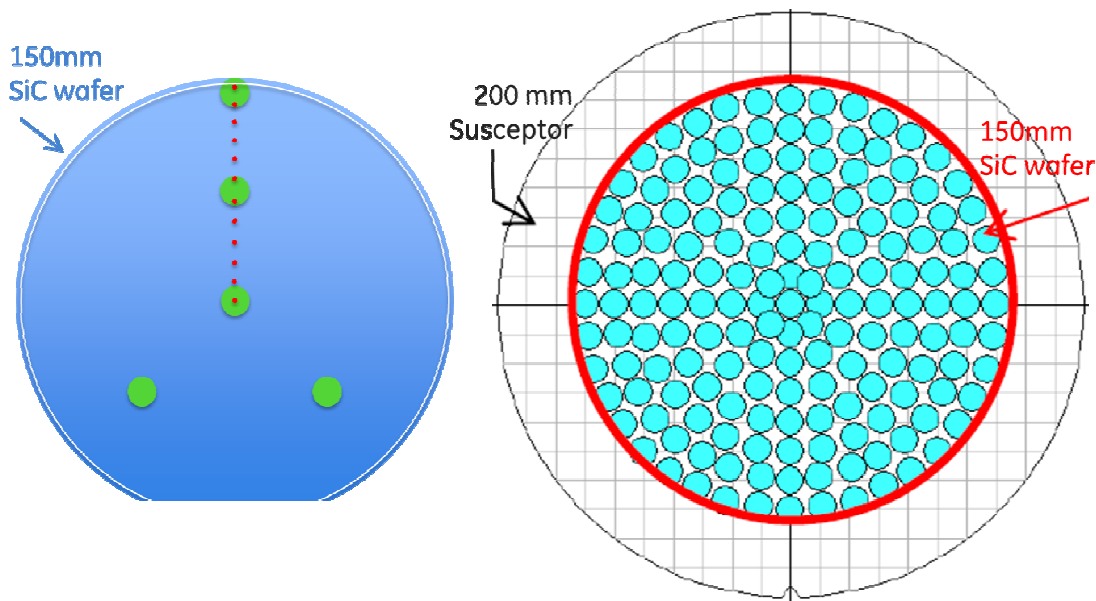


Figure 1. Layout diagrams for some of the patterns used in this study; 150 mm SiC wafers, and ~10 mm diameter TXRF sites shown in both cases (pattern for experiments on 100 mm SiC wafers not shown). Left: 10-point radius scan for MCV (~1.7 mm diameter measurement sites) allows 5-point TXRF measurements to analyze areas contaminated with Hg and areas without. Right: 165-point TXRF measurement on 150 mm 4H SiC wafer shown on 200 mm TXRF susceptor.

Finally, cleaning of wafers was performed in static baths using high-purity quartz ware; bath temperature was controlled to within 1°C via digital readout hotplates. CMOS-grade or higher purity chemicals were used in all cases, and wafers were rinsed in high-purity deionized water. 100 mm wafers were cleaned in a multi-stage clean sequence utilizing sulfuric-peroxide mixture (SPM) with the first stage being segregated as metal-containing, the second stage being a dilute HF dip, and the final step being a second SPM that was segregated as non-metal-containing bath. In separate experiments, 150 mm wafers were split into two clean sequences to compare the combined effects of temperature, concentration, and cleaning time. HF dips utilized here do not change the hydrophilic nature of the SiC surface as previously discussed in (6), and fresh SC1 and SC2 chemistry was used in each clean to avoid issues related to bath life. One sequence on 150 mm SiC wafers included a concentrated RCA process with the SC1 and SC2 mixed in the ratio of 1:1:5, and the another set of cleans on 150 mm SiC wafers utilized a dilute RCA sequence mixed in a ratio of 1:2:50. Process times for the SPM steps were 5

min each, for the concentrated SC1 and SC2 steps the times were 15 min each, and for the dilute SC1 and SC2 the times were 5 min each. The dilute HF step in the dilute RCA sequence was half of the standard time: 30 sec. Process temperature for the concentrated bath sequence was 80°C for SC1 and SC2 but 50°C for the dilute sequence; DHF dip was performed at room temperature in both cases. Wafers sent for post-clean TXRF were aged as long as 10-15 days after MCV. Cleans in this study are representative standard processes for silicon fabrication and are intended to determine whether concentrated chemistry is required to remove contaminants from SiC surfaces.

MCV, Pre-Cleaned TXRF, and Post-Cleaned TXRF Results

All cleans were shown to be effective at removing some degree of the metallic impurities of interest. Mapped Hg levels measured with Mo-anode TXRF on 100 mm SiC wafers were shown to be reduced from a typical average value of 2.5×10^{13} atoms/cm² and typical maximum value of 2.4×10^{14} atoms/cm² immediately after post-epi test, to levels below the 300-second detection limit $\sim 7 \times 10^{10}$ atoms/cm². RCA cleans on 150 mm SiC wafers were shown to be effective at removal of Hg as well as Ni, Fe and other metals, with the post-clean measurements being below the detection limit for the concentrated RCA sequence and lower but still measurable for the dilute RCA sequence.

A comparison of mapped TXRF measurements before and after the dilute RCA clean is exemplified by Figure 2. The surface Fe contaminants are localized near the edges on the wafer before cleans and are still measurable at those locations after the dilute RCA clean, although reduced. The cleaning trend was observable on a variety of metals of interest for yield and reliability concerns (including Hg, Fe, and Ni), and was observed repeatedly on multiple wafers.

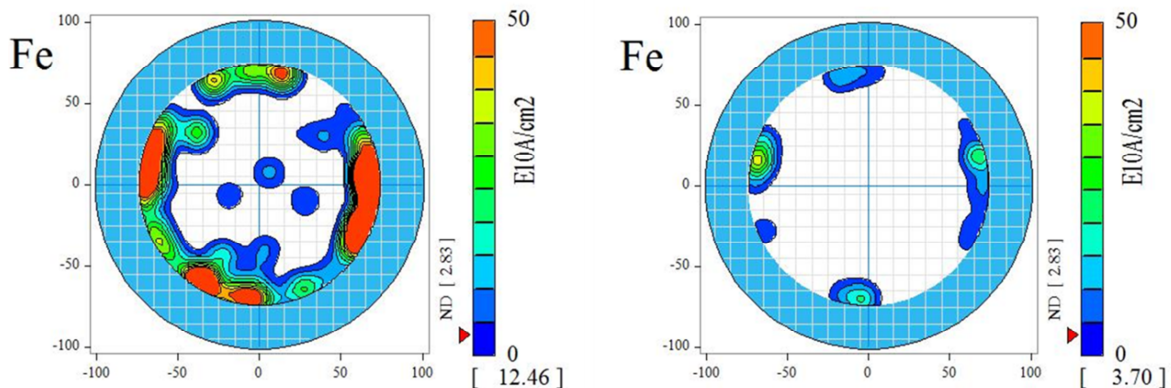


Figure 2. Surface-mapped Fe contamination measured on a 150 mm 4H SiC wafer before and after cleans in a 1:2:50 RCA sequence at 50°C for 5 min per SC1&SC2 bath, DHF was performed for 30 sec. Higher concentration of Fe is noted at the edges at the pre-clean stage, and while all areas exhibit reduction in Fe after cleans, the concentration is still above the detection limit for this process.

The cleaning trend was observable on a variety of metals of interest for yield and reliability concerns (including Ca, Hg, Fe, and Ni) and was observed repeatedly on multiple wafers, although some elements were completely cleaned to values below the

detection limit in TXRF by the dilute RCA (Ti, Cr, Cu, and Zn). Figure 3 illustrates the reduction in surface contamination for Ni using the dilute RCA process. Again, it is noted that concentration of Ni is higher at the wafer edge and that the clean has brought most areas below the detection limit of the measurement.

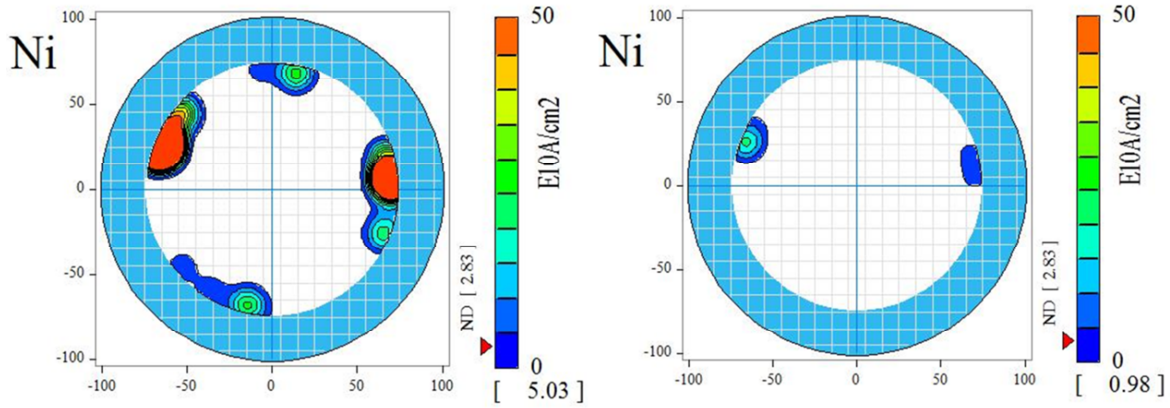


Figure 3. Surface-mapped Ni contamination measured on a 150 mm 4H SiC wafer before and after cleans in a 1:2:50 RCA sequence at 50°C for 5 min per SC1&2 bath, DHF step was performed for 30 sec. Higher concentration of Ni is noted at the edges at the pre-clean stage, and while all areas exhibit reduction in Ni after cleans, the concentration is still above the detection limit in some locations.

Quantified TXRF measurement for Hg, Fe, and Ni in the concentrated bath vs. the dilute process is shown in Table I. The first two rows represent maximum measurements from pre- and post-clean TXRF analysis for the concentrated, longer-time, elevated-temperature process, while the last two rows represent pre- and post-clean measurements for the dilute process run at lower temperature and shorter time. It is clear that even though the typical maximum values are higher on the wafers cleaned in the concentrated chemistry, the post-clean surface contamination is lower in all cases.

TABLE I. Comparison of 15 min, 80°C, concentrated RCA cleans vs. 5 min, 50°C, dilute RCA cleans. Values reported are maximum measurement out of a 165-point mapping TXRF analysis on a 150 mm SiC wafer. A ‘<’ symbol indicates value was below the detection limit of the measurement; in those cases, the detection limit is reported. Maps with edge measurements below the detection limit show that edge artifacts are not an issue for this study.

Pre-clean Hg (at/cm ²)	Pre-clean Fe (at/cm ²)	Pre-clean Ni (at/cm ²)	Clean Process	Post-clean Hg (at/cm ²)	Post-clean Fe (at/cm ²)	Post-clean Ni (at/cm ²)
4.2x10 ¹³	2.6x10 ¹¹	<2.8x10 ¹⁰	1:1:5 RCA	<1.8x10 ¹⁰	<2.8x10 ¹⁰	<2.8x10 ¹⁰
4.2x10 ¹³	5.6x10 ¹¹	6.6x10 ¹²	1:1:5 RCA	<1.8x10 ¹⁰	<2.8x10 ¹⁰	<2.8x10 ¹⁰
7.5x10 ¹²	7.1x10 ¹¹	7.0x10 ¹¹	1:2:50 RCA	2.7x10 ¹⁰	2.9x10 ¹¹	1.3x10 ¹¹
7.6x10 ¹¹	1.7x10 ¹²	3.2x10 ¹²	1:2:50 RCA	1.9x10 ¹⁰	4.3x10 ¹¹	2.4x10 ¹¹

Discussion and Conclusions

Post-clean TXRF showed that a multi-step cleaning process utilizing SPM, DHF, and a second SPM (appropriately segregated) was effective at removing significant Hg

contamination. Similar analysis revealed that concentrated RCA cleans were successful in removing Hg, Fe, and Ni as well as other metallic contaminants from 4H SiC surfaces, while RCA clean run at lower concentration for one third the time at 50°C was not as effective at removing all of these metals. While all post-clean TXRF analyses resulted in lower Hg surface concentrations, the possible effect of evaporation was not considered.

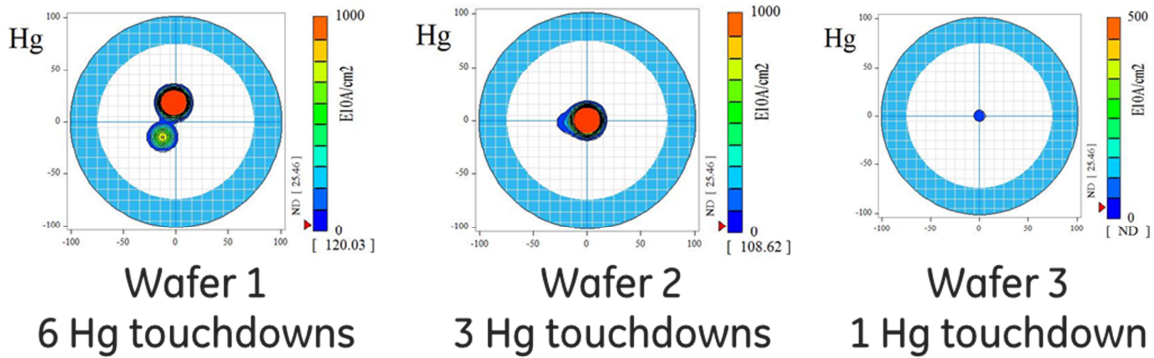


Figure 4. Surface-mapped Hg contamination measured on a 150 mm 4H SiC wafer after various numbers of MCV touchdowns using a 1.7 mm capillary. Maximum values of Hg surface contamination are (from left to right): 4.2×10^{13} atoms/cm², 4.2×10^{13} atoms/cm² and 7.6×10^{11} atoms/cm².

Multiple MCV measurements using a 1.7 mm capillary were required to introduce enough Hg onto the SiC surface to be easily measured in TXRF. This increase was not linearly multiplicative, so it is possible that surface effects, such as adsorption, allow significantly more Hg to be introduced to the surface on subsequent measurements. If this mechanism is true then although the first measurement is at or below the TXRF detection limit, Hg is still present and must be cleaned. Figure 4 illustrates the effect of multiple MCV measurements on SiC wafers; the leftmost panel received a 10-point radial measurement pattern as illustrated in Figure 1, plus 5 additional MCV measurements near the center of the wafer, the wafer from the center panel received the 10-point pattern plus 2 additional measurements, and the rightmost panel illustrates a measurement from the 77-point map. The Hg measurement from the 77-point map was not repeated on a second wafer with an identical pattern, so this measurement could be from summation of multiple localized Hg contamination spots within one TXRF spot. All cleaning approaches reduced the Hg levels. The dilute RCA clean may have been the least effective, as it resulted in the only measurements near the detection limit of 1.9×10^{10} atoms/cm² after cleans. Depending on the requirements for cleanliness, this limit may be acceptable for fabrication.

Since RCA chemistry is known to remove contaminants by oxidizing silicon surfaces and removing those oxides in HF, it is likely that mechanism is not possible on SiC because these chemistries are not expected to etch or oxidize SiC at the temperatures used in this work. It has been suggested in previous work (7) that roughness plays a role in trapping metallic contaminants and that HF treatment results in hydrophilic surfaces largely terminated with Si-OH and C-O groups (6). Results here show that the dilute RCA using shorter time and lower temperature was less effective at removing Fe, Ni, and possibly Hg. While roughness may be a factor, the role of temperature and time could

suggest that dissolution of metals in the SC1 and SC2 chemistries (HCl and NH₄OH) is the dominant mechanism, but we suggest here that diffusion through the Si-OH and C-O surface layers could play a role. It is further noted that the exact mechanism for addition of the Fe and Ni is not known, edge handling from the immersion cassettes and/or contamination from the wafer manufacturing are possible root-causes. Future work exploring the parameters controlling the removal of metallic contaminants is of interest because cost is strongly affected by time (affecting throughput) and by concentration (affecting both material cost and disposal cost) but less by temperature (only affecting initial equipment cost). It will also be desirable to perform this work in equipment capable of spray processing, as high dissolution rates are achievable because of higher flow velocity close to the wafer, which allows faster diffusion of impurities away from the surface (15). This effect has been well evaluated in polymer removal (16) and evaluation on SiC could allow it to be shown relative to metallic contaminants as well, although it is possible that processing in such equipment will result in surface contamination values further below the detection limit of TXRF.

Acknowledgments

Research was sponsored by the NY Power Electronics Manufacturing Consortium. The views and conclusions contained in this document are those of the authors and should not be interpreted as representing the official policies, either expressed or implied, of NY Power Electronics Manufacturing Consortium or the state of New York.

References

1. A. Bolotnikov, P. Losee, G. Dunne, S. Kennerly, B. Rowden, J. Nasadoski, M. Harfman-Todorovic, F. Tao, P. Cioffi, F. Mueller, A. Permuy, L. Stevanovic, "Overview of 1.2 kV – 2.2 kV SiC MOSFETs Targeted for Efficient Operation in Industrial Power Conversion Applications," Applied Power Electronics Conference, (2015).
2. P. Losee, A. Bolotnikov, L. Yu, R. Beaupre, Z. Stum, S. Kennerly, G. Dunne, Y. Sui, J. Kretchmer, A. Johnson, S. Arthur, R. Saia, J. McMahon, D. Lilienfeld, D. Esler, A Gowda, M. Hartig, P. Sandvik, R. Olson, X. Zhu, V. Stolkarts, and L. Stevanovic, "1.2 kV Class SiC MOSFETs with Improved Performance Over Wide Operating Temperature," International Symposium on Power Semiconductor Devices (2014).
3. E. Vivrey, "Wide Band Gap Power Electronics: A Path Toward CO₂ Emission Decrease", Semicon West TechXPOT, (July, 2014).
4. L. Stevanovic et al., "Industrial Readiness of SiC Power Devices", NYS Center for Future Energy Systems (CFES) Annual Conference, (Feb. 2015).
5. M. Liehr, "The New York Power Electronics Manufacturing Consortium at CNSE – SUNY Poly", 2nd IEEE Workshop on Wide Bandgap Power Devices and Applications (WiPDA), (Oct. 2014).
6. S. King, R. Nemanich, and R. Davis, "Wet Chemical Processing of (0001)Si 6H-SiC Hydrophobic and Hydrophilic Surfaces", *J. Electrochem Soc.*, **146** (5) 1910-1917 (1999).

7. M. Madani, Y-L Liu, M. Takahashi, H. Iwasa, and H. Kobayashi, "SiC Cleaning Method by Use of Dilute HCN Aqueous Solutions", *J. Electrochem Soc.*, **155** (11) H895-H898 (2008).
8. M. Kubo, M. Hidaka, M. Kageyama, T. Okano, H. Kobayashi, "Novel Cleaning Method of SiC Wafer with Transition Metal Complex", in: *Silicon Carbide and Related Materials 2011 (ICSCRM 2011)*, ed. R. Devaty, M. Dudley, T. P. Chow and P. Neudeck, **5** 877-880 (2012).
9. K. Danno, H. Saitoh, A. Seki, T. Shirai, H. Suzuki, T. Bessho, Y. Kawai, T. Kimoto, "Diffusion and Gettering of Transition Metals in 4H-SiC", in: *Silicon Carbide and Related Materials 2011 (ICSCRM 2011)*, ed. R. Devaty, M. Dudley, T. P. Chow and P. Neudeck, **3** 225-228 (2012).
10. K. Schuegraf and C. Hu, "Reliability of Thin SiO₂", *Semicond. Sci. Technol.*, **9** 959-1094 (1994).
11. B. Choi and D. Schroder, "Degradation of Ultrathin Oxides by Iron Contamination", *Appl. Phys. Lett.*, **79** (16) 2645-2647 (2001).
12. International Technology Roadmap for Semiconductors, 2000 Update, Front End Process, <http://www.itrs.net>
13. J. Metz, R. Hockett, M. Gil, and S. Tai, "Determination of Contamination from Hg Probe by TXRF Analysis," Electrochemical Society Meeting, (Oct. 1993).
14. H. Kohno, "Evaluation of Contamination of Power Semiconductor Device Wafers by TXRF Spectrometer," *The Rigaku Journal*, 29 (1) 9-14 (2013).
15. G. W. Gale, R. J. Small, K. A. Reinhardt, "Aqueous Cleaning and Surface Conditioning Processes", Chapter 4 in: *Handbook of Silicon Wafer Cleaning Technology*, Second Edition, ed. K. A. Reinhardt and W. Kern, Published by William Andrew, Norwich NY, pg. 249, (2007).
16. C. Hagermoser, S. Henry, E. Rho, J. Song, and H. Kim, in: *Cleaning Technology in Semiconductor Manufacturing IX*, 208th ECS Meeting, Los Angeles, CA, The Electrochemical Society, Pennington NY, pg. 16, (2005).