



Quality Insights

## Patentcloud Quality Insights Annotation Report

*Future Link Systems, LLC v. Qualcomm Inc. et al*

WDTX-6-21-cv-01352

Focus on: U.S. Pat. No. 7,685,439

Filing date: Dec. 22, 2021

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Click on a page number to read

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# Map claims to specification and file wrapper

# Map claims to specification - '439

Which claim terms are or are not in the specification?

Claim Analysis > Claim# 1

Find relevant specification content as intrinsic evidence for claim term interpretation

50 Terms Identified in This Claim [Click to Select Terms](#)

## Select Text

Highlight text from within the claim with your cursor and click on the tooltip "Select Terms" to find references in the Specification.

## Claim# 1

The following claim terms are not literally supported by the specification, which may have rooms for different interpretations.

"arithmetic", "logic", "ALU", "alu", "pulse", "receiving", "ALUs", "alus", "duration", "non-use"

A method for functional control of execution of a program and/or data flow in a **Single Instruction Multiple Data signal processor**

the signal processor having parallel arithmetic and logic functional units ("ALUs") and/or data paths (DPs) for the execution of program instructions and/or data flow, wherein

each ALU and/or DP has at least a gated clock receiving a clock pulse supply,

the signal processor further including a program control unit (PCU),



**Claim Analysis finds these terms in the spec:**

**"Single Instruction Multiple Data signal processor", "clocking signals", "functional units", "data paths", "program control unit", as well as other terms that are highlighted in red.**

# Map claims to specification - '439

Which claim terms are or are not in the specification?

Select Text	Claim# 1
Highlight text from within the claim with your cursor and click on the tooltip "Select Terms" to find references in the Specification.	The following claim terms are not literally supported by the specification, which may have rooms for different interpretations. "arithmetic", "logic", "ALU", "alu", "pulse", "receiving", "ALUs", "alus", "duration", "non-use"
	A method for functional control of execution of a program and/or data flow in a Single Instruction Multiple Data signal processor,
	the signal processor having parallel arithmetic and logic functional units ("ALUs") and/or data paths (DPs) for the execution of program instructions and/or data flow, wherein
	each ALU and/or DP has at least a gated clock receiving a clock pulse supply,
	the signal processor further including a program control unit (PCU).

Review the selected claim element and see how it is defined in the patent specification and related figures.

Selected elements of '439 claim 1

Selected elements of '439 in Spec

Figures of '439

Claim Terms

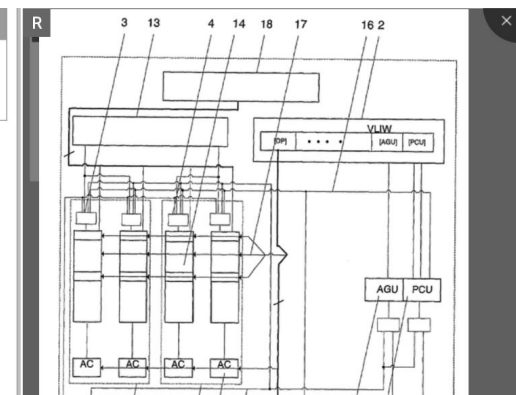
**program**, **control**, **unit** (PCU)

The selected clause includes the following keywords:

- "unit" (1)
- "program" (2)
- "control" (1)

Content

[0018] A further variant of the method involves a halt instruction issued by the **program**, prompting a "software-related halt" state to be triggered by a **Program**, **Control**, **Unit** (PCU) of the signal processor.



# Map claims to specification - '439

Does the allegedly infringing product element fall within or outside the patent's scope?

**Claim Terms**

**program** | **control** | **unit** (PCU)

The selected clause includes the following keywords:

- unit** (1)
- program** (2)
- control** (1)

**Content**

[0018] A further variant of the method involves a halt instruction issued by the **program** prompting a "software-related halt" state to be triggered by a **Program** **Control** **Unit** (PCU) of the signal processor.

With the claim scope interpretation from **Claim Analysis**, verify your findings against the compliant.

Answer the question:

**Does the alleged Invention element fall within or outside the patent's scope?**



**A2.1 Components**

The cluster consists of:

- One to eight cores.
- The DynamIQ Shared Unit (DSU), which connects the cores to an external memory system.

For more information, see the *ARM® DynamIQ® Shared Unit Technical Reference Manual*.

The following figure includes a top-level functional diagram of a core.

\*Optional

**Figure A2-1 Core block diagram**

Claim 1	Accused Products
<p>I[c] the signal processor further including a program control unit (PCU), an interrupt processing unit, and data and program memories, the method comprising:</p>	<p>To the extent the preamble is limiting, in the Accused Products the signal processor further includes a program control unit (PCU), an interrupt processing unit, and data and program memories.</p> <p>For example, in the Snapdragon 730G, each Kryo 470 Silver core further includes a program control unit, an interrupt processing unit, and data and program memories. The program control unit, the data memory, and program memory include, e.g., the data processing unit, the L1 DCache, and L1 ICache of the Kryo 470 Silver core, respectively. Each core also includes an interrupt processing unit, which processes interrupt requests during execution of a program (such as, for instance, interrupts sent to the cores by the general interrupt controller).</p> <p><i>See, e.g.:</i></p>

# Map claims to the file wrapper - '439

Which claim terms are in the file wrapper (i.e. examiner's opinion) ?

## Disclosure Rate by Prior Art

Claim	Disclosure by Single Reference		Disclosure by Multiple References	
	Prosecution History	Post-Grant	Prosecution History	Post-Grant
#1	62%	100%	81%	100%
#2	62%	50%	62%	50%
#3	50%	100%	50%	100%

Claim # 1  
A method for functional control of execution of a program and/or data flow in a Single Instruction Multiple Data signal processor, the signal processor having parallel arithmetic and logic functional units ("ALUs") and/or data paths (DPs) for the execution of program instructions and/or data flow, wherein each ALU and/or DP has at least a gated clock cell input for receiving a clock pulse supply, the signal processor further including a program control unit (PCU), an interrupt processing unit, and data and program memories, the method comprising: receiving at least

Review how the asserted claims were disclosed by the prior art found by the examiner during prosecution and post-grant proceedings.

**A higher percentage means more claim elements were disclosed by the prior art.**

Claim Insights Summary Table > Claim Table (Claim # 1) | Select A Claim 1 2 **switch between claims**

How is each claim element disclosed by cited prior art? Click numbers to find detailed comparison.

**i** The percentage "%" indicates how many keywords in an element being disclosed by a specific references. [Click](#) to find comprehensive explanation of calculation.

**All** Prosecution history Post-Grant  Responded prior arts only

Claims	Prior Art Ref. (4)		
	US5784636	US5918061	US6357016
#1.01 <b>A</b> (100%)	100%	100%	100%
#1.02 <b>A</b> (100%)	100%	100%	100%
#1.03 <b>A</b> (100%)	100%	100%	100%

**Disclosure Rate by Prior Art**

# Map claims terms to the file wrapper - '439

Why was this patent granted? Which claims were amended and how did the scope change?

Claims	Prior Art Ref. (A)	
	US5784636	US5918061
#1.01 (A) (100%)	100%	100%
#1.02 (A) (100%)	100%	100%
#1.03 (A) (100%)	100%	100%
#1.04 (A) (100%)	100%	100%

All of the limitations of this asserted claim element in '439 were 100% known by Nikjou(US5918061).

**Answer the questions:**

***Why was this patent granted?***

Rejection from Examiner

1.01
1.02
1.03
1.04
1.05
1.06
1.07
1.08

Find 6 Result(s) [Find More Result\(s\)](#)

[Filter](#) [Clear All](#)

**Prior Art Ref.** A Nikjou [US5918061]

[20080411-CTFR](#) [Prosecution History](#) [35 U.S.C § 102](#)

Rejection

claim rejections-35 usc § 102 the following is a quotation of the appropriate paragraphs of 35 u.s.c. 102 that form the basis for the rejections under this section made in this office action:a person shall be entitled to a patent unless –(b)the invention was patented or described in a printed publication in this ora foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the united states.

claims 7, 8, and 10 are rejected under 35 u.s.c. 102(b)as being anticipated by **nikjou**, u.s. . patent no.5,918,061(applicant-cited reference).

regarding claim 7, **nikjou** teaches a method for controlling a signal processor(fig.1, soc ], the signal processor having parallel **aii** functional units and/or data paths[dsp cores 15 and 17 ], each with a **gated clock** input for receiving a clock signal, and including a program control unit[microprocessor core 13 ], an interrupt processing unit[col.2, lines 10-12, interrupts can exit the chip from power management modes ], and data and program memories[ram 22.

Remarks

20091207-REM

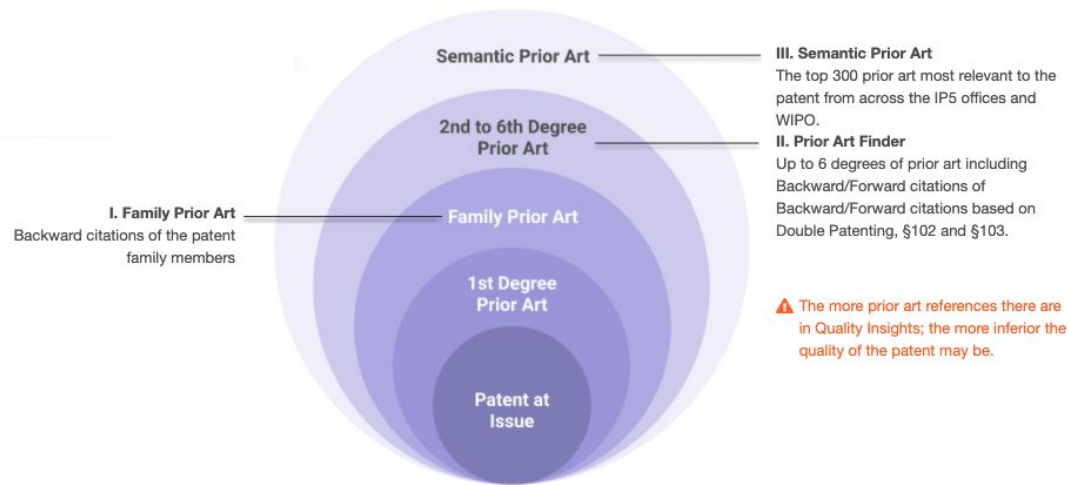
claim r'ccctions 35 u.s.c. 102 the examiner has rejected claims 7, 8, and 10 under 35 u.s.c. § 102 as allegedly being anticipated by u.s. patent no.5,918,061 to **nikjou** (" the **nikjou** reference "). reconsideration and withdrawal are respectfully requested based on the following remarks. applicant has amended claim 7 to include the limitation that the signal processor is a single instruction multiple data signal processor; the **nikjou** reference is directed to an enhanced power managing unit in a multiprocessor chip,( the **nikjou** reference, title), however, the **nikjou** reference fails to disclose or suggest, either alone or in combination with other references of record, "a method for functional control of execution of a program and/or data flow in a single instruction multiple data signal processor," as recited in claim 7 of the instant application in combination with the other elements atty. docket no.a3 6422–pct – usa(066340.021 3)recited therein. in view of the complete absence of this claim limitation in the **nikjou** reference, and thus the fact that the **nikjou** reference does not disclose each and every element of either claim 7, either expressly or inherently, there can be no anticipation of the claimed invention by the **nikjou** reference. accordingly, the rejection under 35 u.s.c. § 102(b) should be withdrawn and claim ' 3' should be allowed.

[^ Show Less](#)

Remark from Applicant



# How does Quality Insights generate prior art?



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# Prior Art Finder

# Prior Art Finder for '439

Review cited and citing patents of '439 from the first to the sixth degree

Filter by:  
 Applicability  
 Legal Basis (102 or 103)  
 Patent Office  
 Legal Status

1st Degree Art <b>3</b>	2nd Degree Art <b>4</b>	N Degree Art <b>36</b>
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## N Degree Art

Extend forward/backward citations from the Second Degree Art

Discover prior art's similarity with claim chart format in seconds !

KEEP Mode

Ranked By : Legal Basis (\$102 first) |

US7685439B2

- 1st Degree (3)
- 2nd Degree (4)
- 3rd Degree (5)
  - US20090201092A1
  - US20170046240A1
  - US20140380081A1
  - US20110075778A1
  - US20140244975A1
- 4th Degree (7)
- 5th Degree (17)
- 6th Degree

4th Degree List | Selected 0/20 Patent(s) [Select top 20 patents in list](#)

	#	Patent No.	Title	Legal Status	Appl. Date	Pub./Issue Date	Assignee (Std)
<input type="checkbox"/>	1	<a href="#">US20120042151A1</a>	PROCESSOR HAVING EXECUTION CORE SE...	Abandoned Appl.	2010-09-10	2012-02-16	SAGER DAVID J
<input type="checkbox"/>	2	<a href="#">US7656235B2</a>	Communication system and oscillation sig...	Active	2007-05-14	2010-02-02	MEDIATEK INC
<input type="checkbox"/>	3	<a href="#">US20190213096A1</a>	FUNCTIONAL UNIT PROMOTION TO MANA...	Abandoned Appl.	2019-03-14	2019-07-11	HEWLETT-PACKARD CO
<input type="checkbox"/>	4	<a href="#">US20130072256A1</a>	Systems and Methods for Reducing Power ...	PGPub - Granted	2011-09-19	2013-03-21	BROADCOM CORP
<input type="checkbox"/>	5	<a href="#">US20190097784A1</a>	Multi-Rate Transceiver Circuitry	PGPub - Granted	2018-10-08	2019-03-28	ALTERA CORP
<input type="checkbox"/>	6	<a href="#">US20050034002A1</a>	Performance control within a multi-process...	PGPub - Granted	2003-08-04	2005-02-10	FLAUTNER KRISZTIAN
<input type="checkbox"/>	7	<a href="#">US20130047166A1</a>	Systems and Methods for Distributing an A...	PGPub - Granted	2011-12-30	2013-02-21	BROADCOM CORP

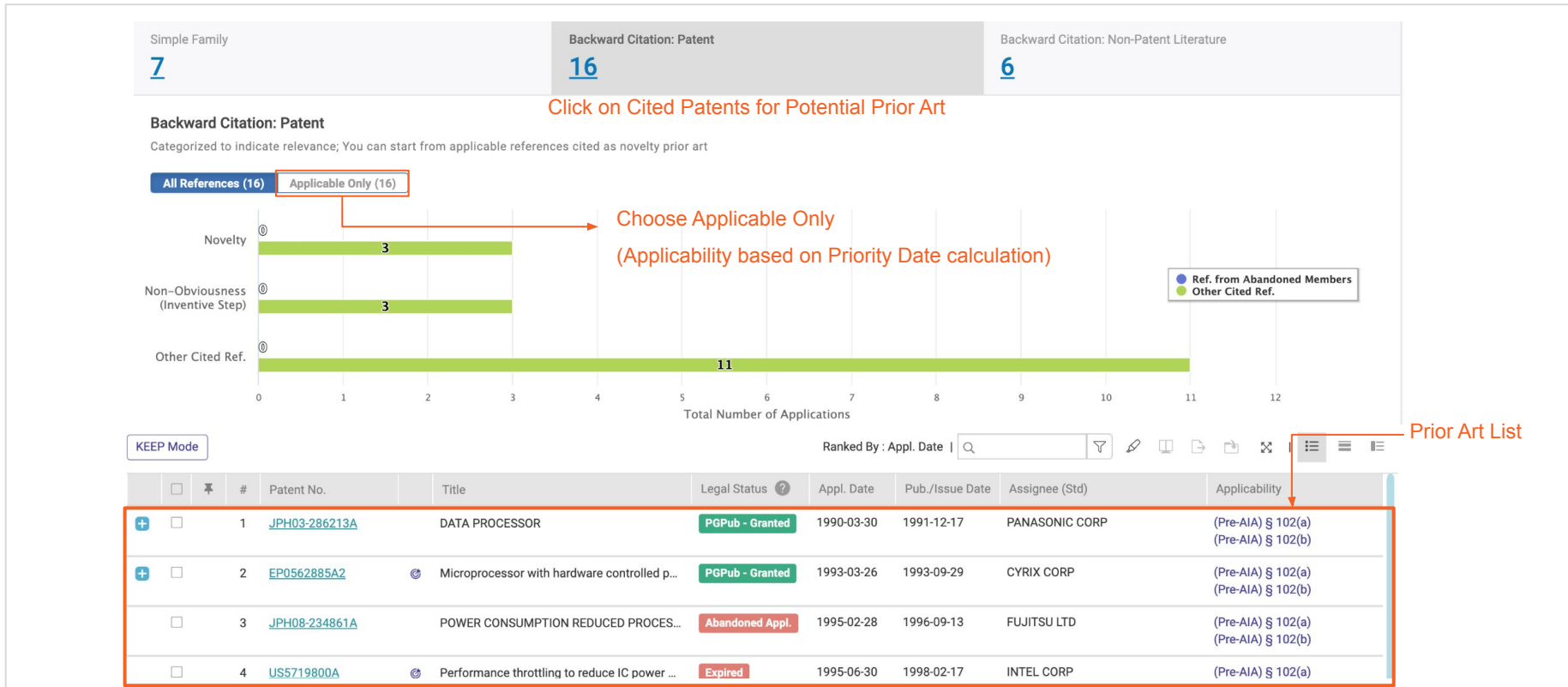
Up to the 6th Degree List

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# Family Prior Art

# Family Prior Art of '439

Review prior art cited by and cited against the family counterparts when available



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# Semantic Prior Art

# Semantic Prior Art of '439

Review potential prior art ranked by concept similarity

Across IP5 and WIPO thanks to Patentcloud's proprietary algorithm

## Semantic Prior Art

Most Relevant US, EP, JP, KR, CN & WO potential prior art references based on **Semantic Similarity** with a patent's first claim and abstract

[Change Scope](#)

Select claim text or enter the desired text/keywords

Discover prior art's similarity with claim chart format in seconds !

KEEP Mode 0 are of high semantic similarity

Ranked By : Relevance

<input type="checkbox"/>		Ranking	Patent No.		Title	Legal Status	Appl. Date	Pub./Issue Date	Assignee (Std)	Applicability
<input type="checkbox"/>		1	<a href="#">US20020004916A1</a>		Methods and apparatus for power control i...	<b>PGPub - Granted</b>	2001-05-11	2002-01-10	MARCHAND PATRICK R	+2 (Pre-AIA) § 102(a) (Pre-AIA) § 102(b) (Pre-AIA) § 102(e)(1)
<input type="checkbox"/>		2	<a href="#">US6564328B1</a>		Microprocessor with digital power throttle	<b>Expired</b>	1999-12-23	2003-05-13	INTEL CORP	(Pre-AIA) § 102(e)(2)
<input type="checkbox"/>		3	<a href="#">JPH08-234861A</a>		POWER CONSUMPTION REDUCED PROCES...	<b>Abandoned</b>	1995-02-28	1996-09-13	FUJITSU LTD	(Pre-AIA) § 102(a) (Pre-AIA) § 102(b)
<input type="checkbox"/>		4	<a href="#">JPH03-286213A</a>		DATA PROCESSOR	<b>PGPub - Granted</b>	1990-03-30	1991-12-17	PANASONIC CORP	(Pre-AIA) § 102(a) (Pre-AIA) § 102(b)
<input type="checkbox"/>		5	<a href="#">WO1999/014685A1</a>		DATA PROCESSOR AND DATA PROCESSIN...	<b>Abandoned</b>	1997-09-16	1999-03-25	HITACHI LTD	(Pre-AIA) § 102(a) (Pre-AIA) § 102(b)
<input type="checkbox"/>		6	<a href="#">JPH09-200026A</a>		LSI LOGIC CIRCUIT	<b>Abandoned</b>	1996-01-22	1997-07-31	OKI ELECTRIC IND CO LTD	(Pre-AIA) § 102(a) (Pre-AIA) § 102(b)
<input type="checkbox"/>		7	<a href="#">EP0799446A1</a>		MICROPROCESSOR FOR SIMULTANEOUS E...	<b>Abandoned</b>	1995-12-20	1997-10-08	MOTOROLA INC	(Pre-AIA) § 102(a) (Pre-AIA) § 102(b)
<input type="checkbox"/>		8	<a href="#">US20030005264A1</a>		Device and method for control of the data s...	<b>Abandoned</b>	2002-06-28	2003-01-02	DRESCHER WOLFRAM	+1 (Pre-AIA) § 102(e)(1)

# Semantic Prior Art of '439

Review potential prior art ranked by concept similarity

Active

Download Report
Save Report

## US7685439B2 [🔗](#)

Method for effecting the controlled shutdown of data processing units

Overview
History
Claim Analysis
Claim Insights
Family Prior Art
Prior Art Finder
Semantic Prior Art
File Wrapper Search

📘 About Semantic Prior Art

### Semantic Prior Art

Most Relevant US, EP, JP, KR, CN & WO potential prior art references based on [Semantic Similarity](#) within the scope below. [🔄 Reset to Default](#)

+ Add text from claims
Submit

🔗 Discover prior art's similarity with claim chart format in search results

Add text from claims
✕

Select A Claim

1
2
3
4
5
6

A method for functional control of execution of a program and/or data flow in a Single Instruction Multiple Data signal processor, the signal processor having parallel arithmetic and logic functional units ("ALUs") and/or data paths (DPs) for the execution of program instructions and/or data flow, wherein each ALU and/or DP has at least a gated clock cell input for receiving a clock pulse supply, the signal processor further including a program control unit (PCU), an interrupt processing unit, and data and program memories, the method comprising: receiving at least one of a hardware-

Add

✍️ adding text from claims to find more related Prior Art



---

# Comparison tools

# Prior Art Comparison (claim chart format)

What does this prior art say about the critical elements?

1.01
1.02
1.03
1.04
1.05
1.06
1.07
1.08

Find **15** Result(s) | Disclosure Rate : **50%**

Disclosure Rate of Prior Art

### Claim Element

#1.03 each **ALU** and/or **DP** has at least a **gated clock cell** input for receiving a **clock pulse supply**.

**Keyword List** ⓘ

- 👁
alu (17)
 FW
PA
- 👁
supply
supplied (2)
 FW
PA
- 👁
gated clock (1)
 FW
PA
- 👁
clock pulse (0)
 FW
- 👁
dp (0)
 FW

### US20020004916A1 Content

Specification

**[17]** [ 0017 ] FIG . 3B illustrates an exemplary set of port usage control logic with **gated clock** address latches in accordance with the present invention ;

**[19]** [ 0019 ] FIG . 5A illustrates an exemplary ManArray **ALU** instruction encoding with specific fields identified ;

**[20]** [ 0020 ] FIG . 5B illustrates an exemplary ManArray **ALU** ADD syntax / operation table for the instruction of FIG . 5A .

**[28]** [ 0028 ] In the exemplary system 100 , common elements are used throughout to simplify the explanation , though actual implementations are not limited to this restriction . For example , the execution units 131 in the combined SP / PE0 101 can be separated into a set of execution units optimized for the control function , for example , fixed point execution units in the SP , and the PE0 as well as the other PEs can be optimized for a floating point application . For the purposes of this description , it is assumed that the execution units 131 are of the same type in the SP / PE0 and the PEs . In a similar manner , SP / PE0 and the other PEs use a five instruction slot iVLIW architecture which contains a VLIW memory ( VIM ) 109 and an instruction decode and VIM controller functional unit 107 which receives instructions as dispatched from the SP / PE0 ' s I - fetch unit 103 and generates VIM addresses and control signals 108 required to access the iVLIWs stored in the VIM . Referenced instruction types are identified by the letters SLAMD in VIM 109 , where the letters are matched up with instruction types as follows : Store ( S ) , Load ( L ) , **ALU** ( A ) , MAU ( M ) , and DSU ( D ) .

**[37]** [ 0036 ] A reconfigurable register file with port address latches and port usage control logic system 200 as used in each PE and SP of FIG . 1 is shown in FIG . 2B for a subset of only one execution unit , the **ALU** , from the multi - execution units shown in the PEs of FIG . 1 . Expansion with additional execution units is discussed further below . In FIG . 2B , an instruction is received into an instruction register 206 which controls the operation for that PE or SP . This instruction register 206 can be loaded with one of the

**Answer the question:**  
**What does this prior art say about the Claim elements: "ALU" ?**

**Discover prior art similarity with keywords (includes keyword stemming) mapped to the selected prior art reference Abstract, Claims, and Specification.**

# Prior Art Comparison (sample output)

Easily generate a table like below

Claim		Claim-Term Interpretation	Semantic Prior Art - '916	3rd Degree Citation Prior Art - B
1	A method for functional control of execution of a program and/or data flow in a Single Instruction Multiple Data signal processor,	Refer to Claim Analysis results	80%	.....
	the signal processor having parallel arithmetic and logic functional units ("ALUs") and/or data paths (DPs) for the execution of program instructions and/or data flow, wherein	.....	50%	.....
	each ALU and/or DP has at least a gated clock cell input for receiving a clock pulse supply,	.....	50%	
	.....switching off the clock supply of particular ALUs and/or DPs of the signal processor that are not being used for the program execution and/or data flow for the duration of their non-use.	.....	.....	

System-identified keywords and key phrases  
(highlighting of other keywords is available)

Results from claim to specification  
and file wrapper mapping

Results from prior art comparison  
by claim element

---

# Prior art downloads

# Prior art downloads

Select all

Export

#	Patent No.	Title
<input checked="" type="checkbox"/>	1 CN1247662A	Dual use spea
<input checked="" type="checkbox"/>	2 EP0998105B1	Mobile teleph
<input checked="" type="checkbox"/>	3 JPH09-036932A	EXTERNAL RI
<input checked="" type="checkbox"/>	4 JPH11-055358A	MOBILE RAD
<input checked="" type="checkbox"/>	5 US5317622	Ringling circuit for use in a telephone set f... <span>Abandoned</span> 1994-05-31 1993-02-23 NEC CORP



Download patent data in Excel or PDF format for Family Prior Art, Second Degree Prior Art, and/or Semantic Prior Art.

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# Prosecution and PTAB History

## Key Events

# Key Events - '439

1 Prosecution & 1 Post-Grant

Event History

**2**

Family Status

**7** Applications

Prior Art Status

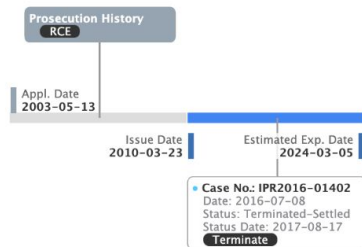
**370** Applications / **6** NPL References

Event History | **1** Prosecution History / **1** Post-Grant

Validity challenges to a patent in its prosecution history and post-grant events

# of Family Counterparts and Legal Status

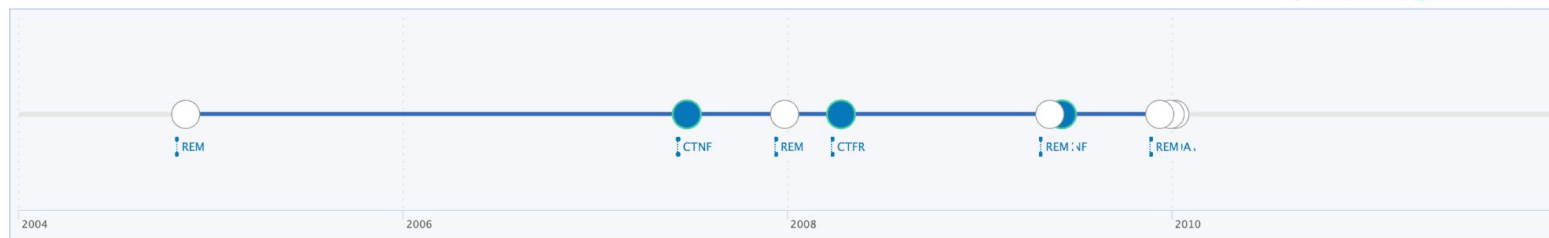
# of Highly Relevant Prior Art References



Legend	
Document Code	Document Description
CTFR	Final rejection
CTNF	Non-final rejection
CLM	Claims
REM	Remarks

Other Document  Rejection Document

Timeline of Prosecution:



# Key Events - '439

## Prosecution History

**10/514850 Prior Art Ref.** | 1 Ref.

Check prior art cited and the legal basis of these challenges

**Double Patenting** | 0 Ref.

**§ 102** | 1 Ref.

[US5918061](#)  
Nikjou

**§ 103** | 0 Ref.

**Summary of 10/514850 History** | 10 Event(s)

Clickable events for original OAs and their OCR version when available.

Direct links to Grounds, Claims Highlighted and Prior Art Details

Data Last Updated on: 2021-11-13

Descriptions (Code)	Date	Prior Art Ref.
Notice of Allowance (NOA)	2010-01-05	
Notice of Allowance (NOA)	2009-12-28	
Applicant Arguments/Remarks Made in an Amendment (REM)	2009-12-07	
<a href="#">Claims (CLM)</a>		
<b>Non-Final Rejection (CTNF)</b>	2009-06-05	Grounds 2 ^
Legal Basis	Claims	Prior Art Ref.
35 U.S.C. § 102	claim 7,8,10	Nikjou US5918061
35 U.S.C. § 112	claim 7,8,9,10,11,12	
Request for Continued Examination (RCEX)	2009-05-13	
Applicant Arguments/Remarks Made in an Amendment (REM)	2009-05-13	



# Key Events - '439

Post-Grant

Event History

**2**

Family Status

**7** Applications

Prior Art Status

**370** Applications / **6** NPL References

Event History | **1** Prosecution History / **1** Post-Grant

# of Family Counterparts and Legal Status

# of Highly Relevant Prior Art References

Validity challenges to a patent in its prosecution history and post-grant events

Prosecution History

RCE

Appl. Date  
2003-05-13

Issue Date  
2010-03-23

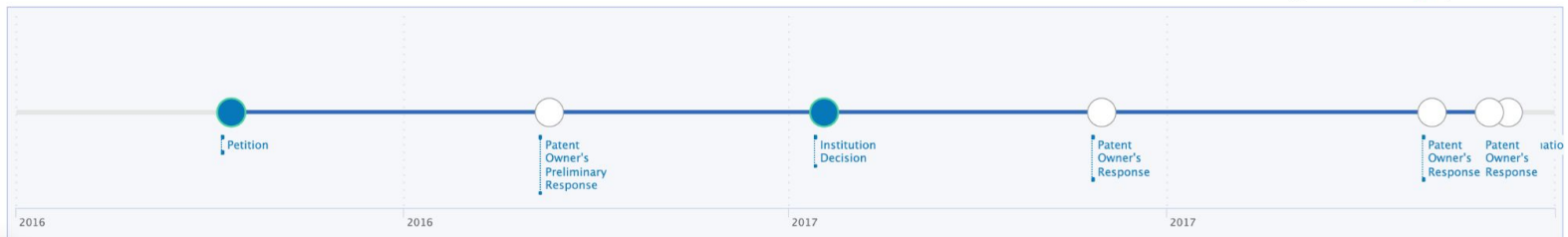
Estimated Exp. Date  
2024-03-05

Click to view each event in summary and details of IPR

• Case No.: IPR2016-01402  
Date: 2016-07-08  
Status: Terminated-Settled  
Status Date: 2017-08-17  
Terminate

Timeline of IPR:

○ Other Document ● Rejection Document



# Key Events - '439

## Prosecution History

IPR2016-01402 Prior Art Ref. | 4 Ref.

Check prior art cited and the legal basis of these challenges

Double Patenting | 0 Ref.

§ 102 | 1 Ref.

[US5918061](#)  
Nikjou

§ 103 | 3 Ref.

[US5918061](#) (1st)  
Nikjou

[US5784636](#)  
Rupp

[US6357016](#)  
Rodgers

→ Clickable events for original OAs and their OCR version when available.

### Order

ORDERED that pursuant to 35 U.S.C. § 314, an inter partes review is hereby instituted as to claims 1 and 4 under 35 U.S.C. § 103(a) as obvious over Nikjou and Rodgers;  
 FURTHER ORDERED that no other grounds are authorized for this inter partes review other than those specifically identified above; and  
 FURTHER ORDERED that pursuant to 35 U.S.C. § 314(d) and

Summary of IPR2016-01402 History | 7 Event(s)

Direct links to Grounds, Claims Highlighted and Prior Art Details

Data Last Updated on: 2021-11-15

Descriptions (Code)	Date ↓	Prior Art Ref.
Termination	2017-08-17	
Patent Owner's Response	2017-08-11	
Patent Owner's Response	2017-07-24	
Patent Owner's Response	2017-04-10	
Institution Decision	2017-01-12	Grounds 3 ^
Legal Basis	Claims	Prior Art Ref.
35 U.S.C. § 102	claim 7,8,10,12	Nikjou US5918061

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# Prosecution and PTAB History Search

# Patent File Wrapper Search

Directly discover details in the prosecution history and post-grant proceeding across all documents via a keyword search.

### Cross-Document Search

Enter keyword to find documents including specific legal basis or specific claim terms

[About File Wrapper Search](#)

**Rejections, Remarks, and Notice of Allowance in Prosecution History** | 13 Records [↓](#)

<input type="checkbox"/> Descriptions (Code) <a href="#">?</a>	Party	Date <a href="#">?</a>
<input type="checkbox"/> Notice of Allowance (NOA)	USPTO	2015-09-24
<input type="checkbox"/> Applicant Arguments/Remarks Made in an Amendment (REM)	Applicant	2015-06-19
<input type="checkbox"/> Non-Final Rejection (CTNF)	USPTO	2015-03-19
<input type="checkbox"/> Request for Continued Examination (RCEX)	Applicant	2015-03-03
<input type="checkbox"/> Applicant Arguments/Remarks Made in an Amendment (REM)	Applicant	2015-03-03
<input type="checkbox"/> Final Rejection (CTFR)	USPTO	2014-11-03
<input type="checkbox"/> Applicant Arguments/Remarks Made in an Amendment (REM)	Applicant	2014-10-15
<input type="checkbox"/> Non-Final Rejection (CTNF)	USPTO	2014-07-15
<input type="checkbox"/> Request for Continued Examination (RCEX)	Applicant	2014-06-26
<input type="checkbox"/> Applicant Arguments/Remarks Made in an Amendment (REM)	Applicant	2014-06-26
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<input type="checkbox"/> Applicant Arguments/Remarks Made in an Amendment (REM)	Applicant	2014-02-07
<input type="checkbox"/> Non-Final Rejection (CTNF)	USPTO	2013-11-07

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# Prosecution and PTAB History PDF Downloads

# PDF Downloads

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### Cross-Document Search

Enter keyword to find documents including specific legal basis or specific claim terms

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**Rejections, Remarks, and Notice of Allowance in Prosecution History** | 13 Records ↓

<input type="checkbox"/> Descriptions (Code) <span style="font-size: small;">?</span>	Party	Date <span style="font-size: small;">?</span>
<input type="checkbox"/> Notice of Allowance (NOA)	USPTO	2015-09-24
<input type="checkbox"/> Applicant Arguments/Remarks Made in an Amendment (REM)	Applicant	2015-06-19
<input type="checkbox"/> Non-Final Rejection (CTNF)	USPTO	2015-03-19
<input type="checkbox"/> Request for Continued Examination (RCEX)	Applicant	2015-03-03
<input type="checkbox"/> Applicant Arguments/Remarks Made in an Amendment (REM)	Applicant	2015-03-03
<input type="checkbox"/> Final Rejection (CTFR)	USPTO	2014-11-03
<input type="checkbox"/> Applicant Arguments/Remarks Made in an Amendment (REM)	Applicant	2014-10-15
<input type="checkbox"/> Non-Final Rejection (CTNF)	USPTO	2014-07-15
<input type="checkbox"/> Request for Continued Examination (RCEX)	Applicant	2014-06-26
<input type="checkbox"/> Applicant Arguments/Remarks Made in an Amendment (REM)	Applicant	2014-06-26
<input type="checkbox"/> Final Rejection (CTFR)	USPTO	2014-02-26
<input type="checkbox"/> Applicant Arguments/Remarks Made in an Amendment (REM)	Applicant	2014-02-07
<input type="checkbox"/> Non-Final Rejection (CTNF)	USPTO	2013-11-07

Data Last Updated on 2021-04-08

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# Prosecution and PTAB History Side-by-side PDF and OCR

# Side by Side: PDF & OCR



Conduct a keyword search in a single document to identify the claim scope quickly and easily. You can even search additional claim terms within rejections.

The screenshot displays a software interface for keyword searching. On the left, a 'Keywords (2)' panel is highlighted with an orange box. It contains a 'Select a Keyword Set' dropdown, a 'Clear All' button, and two keyword entries: 'sensor' (33) and 'flexible substrate (1)'. Below these is an '+ Add new keyword' button and a 'Save to Keyword Set' button at the bottom.

The main area shows a side-by-side comparison of a patent document (left) and its OCR output (right). The document is titled 'U9926311B2 - CTNF [2015-03-19]' and is page 5 of 18. The document text includes:

Application/Control Number: 13/284,674 Page 5  
 Art Unit: 2867

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the touch panel taught by Grant by adding drive or sense electrodes made of flexible conductive material as taught by Hotelling since the sensor traces provide level shifting from a low voltage level to a higher voltage level, thus providing a better signal-to-noise ratio for improved noise reduction purposes while the drive traces provide shielding for the sense traces.

Neither Grant nor Hotelling specifically teach wherein the flexible conductive material of the drive or sense electrodes comprises first and second conductive lines that electrically contact one another at an intersection.

However, Gray does teach wherein the flexible conductive material of the drive or sense electrodes comprises first and second conductive lines that electrically contact one another at an intersection (Fig. 2; [0063]: **A number of conductors forming rows and columns of a conductive pattern (e.g., indium tin oxide (ITO)) may be deposited on a substrate composed of polyester or other material on one or more layers of the touchscreen... the row and column oriented conductors may be disposed on the same layer...**; See also Miller US 5,089,672; Col. 2, lines 11-16; Col. 5, lines 1-20; Col. 5, lines 61-68).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the combination of Grant and Hotelling by including the conductive lines (rows and columns) taught by Gray for the purpose of "providing paths for signals traveling through the touchscreen" (See Gray; Abstract).

The OCR output on the right mirrors the document text but includes search results for the keywords 'sensor' and 'flexible substrate'. For example, it highlights 'flexible substrate' in the text and provides a list of corresponding descriptions: [0003], [0006], [0006], [0022], [0023], [0027], and [0071]. It also identifies 'flexible circuitry' and 'capacitive touch sensor' as flexible conductive material.





## QI is a Game Changer

- Take control of a patent at issue with its comprehensive Overview
- Discover claim construction issues and define the claim scope
- Find more relevant prior art references
- Save time to increase productivity for a pitch and win