



Quality Insights

## Patentcloud *Quality Insights* Annotation Report

*Qualcomm Incorporated v. Monterey Research, LLC*

PTAB-IPR2020-00130

Focus on: U.S. Pat. No.6,459,625

Filing date: Nov. 05, 2021

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Click on a page number to read

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# Map claims to specification and file wrapper

# Map claims to specification - '625

Which claim terms are or are not in the specification?

**Select Text**

Highlight text from within the claim with your cursor and click on the tooltip "Select Terms" to find references in the Specification.

28 Terms Identified in This Claim [Click to Select Terms](#)

**Claim# 1**

The following claim terms are not literally supported by the specification, which may have rooms for different interpretations.  
"direction", "number"

**Select Terms**

A method of **electrically interconnecting** a **periphery area** in a **flash memory** comprising:

providing a plurality of **sub-circuits fabricated** in a **periphery area** of a **silicon substrate**, wherein

each **sub-circuit** includes at least one **electrical circuit** having a plurality of **circuit components**;

**partially electrically interconnecting** said **circuit components** with a first **metal interconnect layer** including a plurality of first **metal layer lines** that are **oriented substantially** in one direction;

**completing** the **electrical interconnection** of said **circuit components** in each **respective sub-circuit** with a second **metal interconnect layer** including a plurality of second **metal layer lines** that are **oriented substantially perpendicular** to said first **metal layer lines**;



*Claim Analysis* finds these terms in the spec:  
**"periphery area", "flash memory", "silicon substrate", "sub-circuit"**, as well as other terms that are highlighted in red.

# Map claims to specification - '625

Which claim terms are or are not in the specification?

**Select Text**

Highlight text from within the claim with your cursor and click on the tooltip "Select Terms" to find references in the Specification.

Claim# 1
<p>The following claim terms are not literally supported by the specification, which may have rooms for different interpretations.</p> <p>"direction", "number"</p>
<p>A method of electrically interconnecting a <span style="background-color: #d3d3d3;">periphery area in a flash memory</span>, comprising:</p>
<p>providing a plurality of sub-circuits fabricated in a periphery area of a silicon substrate, wherein</p>
<p>each sub-circuit includes at least one electrical circuit having a plurality of circuit components;</p>
<p>partially electrically interconnecting said circuit components with a first metal interconnect layer including a plurality of first metal layer lines that are oriented substantially in one direction;</p>

Review the selected claim element and see how it is defined in the patent specification and related figures.

Selected elements of '625 claim 1

Selected elements of '625 in Spec

Figures of '625

**Claim Terms**

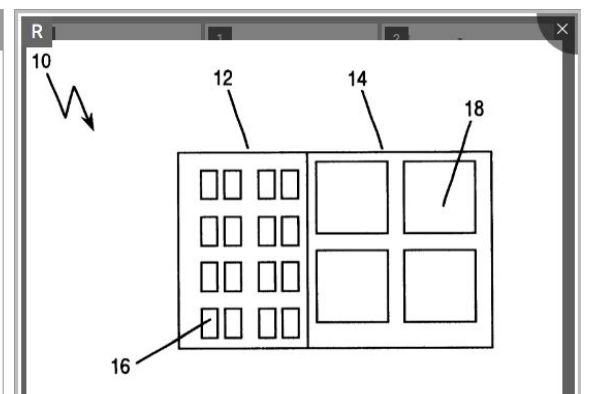
periphery area in a flash memory

The selected clause includes the following keywords:

- memory (62)
- flash (43)
- area (70)
- periphery (36)

**Content**

[0007] A known problem with this method and system of electrical connection is layout area consumed by routing channels of the first and second layer of metal between the sub-circuits in the periphery area. In addition, layout area is consumed for routing channels that are used to route the first and second metal layers between the electrical components that form the sub-circuits. The layout area for the routing channels required by existing electrical connection systems and methods increases the size of the periphery area on the flash memory. The area on the flash memory that is not consumed by the periphery area can be reserved for the core cell area, allowing more core memory cells to be fabricated on the flash memory. It is therefore desirable to minimize the amount of periphery area consumed, thereby increasing



# Map claims to specification - '625

Does the allegedly infringing product element fall within or outside the patent's scope?

**Claim Terms**

`periphery area` in a `flash memory`

The selected clause includes the following keywords:

- `memory` (62)
- `flash` (43)
- `area` (70)
- `periphery` (36)

**Content**

[0007] A known problem with this method and system of electrical connection is layout `area` consumed by routing channels of the first and second layer of metal between the sub-circuits in the `periphery area`. In addition, layout `area` is consumed for routing channels that are used to route the first and second metal layers between the electrical components that form the sub-circuits. The layout `area` for the routing channels required by existing electrical connection systems and methods increases the size of the `periphery area` on the `flash memory`. The `area` on the `flash memory` that is not consumed by the `periphery area` can be reserved for the core cell `area` allowing more core `memory` cells to be fabricated on the `flash memory`. It is therefore desirable to minimize the amount of `periphery area` consumed, thereby increasing the amount of information stored in the `flash memory`.

With the claim scope interpretation from **Claim Analysis**, verify your findings against the petition.

Answer the question:

**Does the alleged Invention element fall within or outside the patent's scope?**

Claim	Preamble	Body
1	"a periphery area in a flash memory"	"a periphery area of a silicon substrate"
6	"in a flash memory"	"a periphery area of a silicon substrate"
10	"a periphery area in a memory device"	"a periphery area of a silicon substrate"

Petitioner argues that the phrase "a periphery area of a silicon substrate," as recited in the body of each of claims 1, 6, and 10, should be construed as limited by the preamble of each respective claim. Pet. 20–23. According to Petitioner, "Claims 1 and 6 should be limited to periphery areas of flash memory, and Claim 10 should be limited to periphery areas of a memory device." *Id.* at 22; *see id.* at 20–21. In support of this argument, Petitioner contends that, similar to *Deere v. Bush Hog*,

# Map claims to the file wrapper - '625

Which claim terms are in the file wrapper(i.e. examiner's opinion) ?

Disclosure Rate by Prior Art

Claim	Disclosure by Single Reference		Disclosure by Multiple References	
	Prosecution History	Post-Grant	Prosecution History	Post-Grant
<input checked="" type="checkbox"/> #1	0%	100%	0%	100%
<input checked="" type="checkbox"/> #6	0%	83%	0%	83%
<input checked="" type="checkbox"/> #10	0%	77%	0%	77%

Confirm

Review how the asserted claims were disclosed by the prior art found by the examiner during prosecution and post-grant proceedings.

**A higher percentage means**  
more claim elements were disclosed by the prior art.

Claim Insights Summary Table > Claim Table (Claim# 1) | Select A Claim 1 6 10 switch between claims

How is each claim element disclosed by cited prior art? Click numbers to find detailed comparison.

**1** The percentage "%" indicates how many keywords in an element being disclosed by a specific references.  
[Click](#) to find comprehensive explanation of calculation.

**All** Prosecution history Post-Grant ☐ Responded prior arts only

Claims	Prior Art Ref. (4)			
	POSITA	JPH11-68066	US5847420	OTHER REFERENCE
#1.01 (100%)	66%	66%	100%	100%
#1.02 (100%)	40%	0%	100%	100%
#1.03 (100%)	0%	50%	100%	0%
#1.04 (100%)	0%	71%	100%	71%

Disclosure Rate by Prior Art

# Map claims terms to the file wrapper - '625

How was this patent challenged during Prosecution & IPR?

Claims	Prior Art Ref. (4)		
	POSITA	JPH11-68066	US5847420
#1.01 (100%)	66%	66%	100%
#1.02 (100%)	40%	0%	100%
#1.03 (100%)	0%	50%	100%
#1.04 (100%)	0%	71%	100%
#1.05 (100%)	0%	50%	100%
#1.06 (100%)	0%	44%	100%

All of the limitations of this asserted claim element in '625 were 100% known by (US5847420).

**Answer the questions:**

**How was this patent challenged during IPR?**

Petition from Applicant

Find 1 Result(s) [Filter](#) [Clear All](#)

Prior Art Ref. '420 [US5847420]

[Petition](#) [20131108-Petition](#) [IPR2014-00104](#) [35 U.S.C. § 103](#) [35 U.S.C. § 102](#)

Claim Element

#1.02 providing a plurality of sub-circuits fabricated in a periphery area of a silicon substrate, wherein

the '420 reference discloses each and every limitation of claims 1-14 of the '625 patent claim 1 requires(a)providing a plurality of sub-circuits fabricated in a periphery area of a silicon substrate, wherein each sub-circuit includes at least one electrical circuit having a plurality of circuit components ;(b)partially electrically interconnecting said circuit components with a first metal interconnect layer including a plurality of first metal layer lines that are oriented substantially in one direction ;(c)completing the electrical interconnection of said circuit components in each respective sub-circuit with a second metal interconnect layer including a plurality of second metal layer lines that are oriented substantially perpendicular to said first metal layer lines;and(d)electrically interconnecting each respective sub- petition for inter partes review(ipr2014-00104)circuit with a predetermined number of other sub-circuits with a third metal interconnect layer including a plurality of third metal layer lines.

independent claims 1, 6, and 10 of the '625 patent are directed to the same subject matter with minor variations.

claim 1 requires that the first and second metal interconnect layers be perpendicular to each other, but does not specify a physical relationship between the second and third metal interconnect layers.

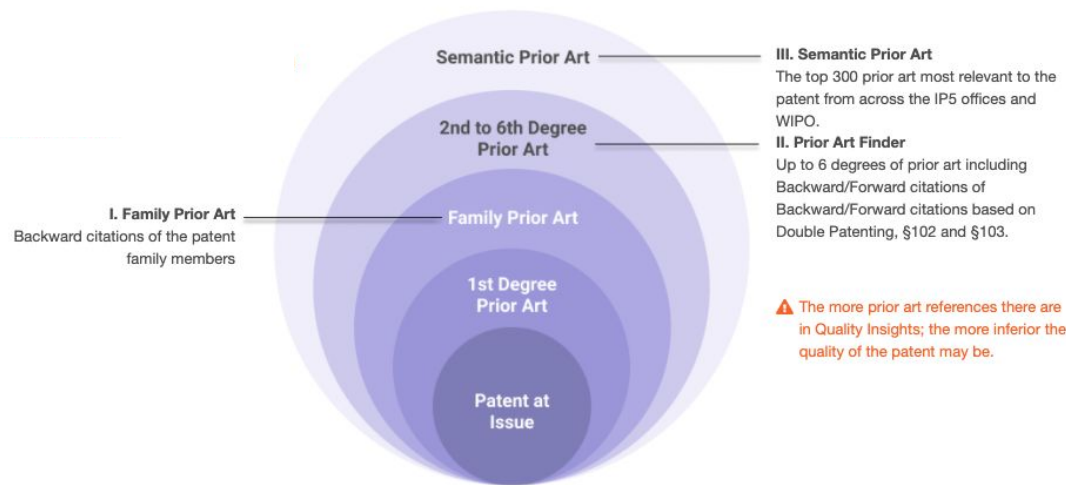
claims 6 and 10, however, require the first and second metal interconnect layers to be substantially perpendicular and also require the first and third metal interconnect layers to be substantially parallel.

claim 6 also differs from claim 1 in that it recites that each sub-circuit includes at least one electrical circuit having rows of transistors.

all the features of claim 1 are disclosed by the '420 reference .. mack decl.at ¶ 55 .. for example, as explained above, the '420 reference discloses nmos and pmos transistors in nmos and pmos regions in the periphery area .. mx625-1001 at fig.13(region x); fig.15(showing details of region x;most of the specification is directed to describing structures in x, see i d.7:15-17) .. the transistors are used to form functional circuits in the periphery .. as explained above, the '420 reference describes that the first metal layer, w, is used to connect transistors to partially connect one or



# How does Quality Insights generate prior art?



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# Prior Art Finder

# Prior Art Finder for '625

Review cited and citing patents of '625 from the first to the sixth degree

Filter by:  
 Applicability  
 Legal Basis (102 or 103)  
 Patent Office  
 Legal Status

1st Degree Art  
**3**

2nd Degree Art  
**6**

N Degree Art  
**69**

**N Degree Art**  
 Extend forward/backward citations from the Second Degree Art

Discover prior art's similarity with claim chart format in seconds !

KEEP Mode

Ranked By : Legal Basis (§102 first) |

**US6459625B1**  

1st Degree (3)  
2nd Degree (6)  
US20060022705A1  
US20050117436A1  
US6823499B1  
US20060164121A1  
US20030144760A1  
US20060028241A1  
3rd Degree (20)  
4th Degree (20)  
5th Degree (20)  
6th Degree

2nd Degree List | Selected 0/20 Patent(s) [Select top 20 patents in list](#) [Confirm](#)

	#	Patent No.	Title	Legal Status	Appl. Date	Pub./Issue Date	Assignee (Std)
<input type="checkbox"/>	1	<a href="#">US20060022705A1</a>	Structured integrated circuit device	PGPub - Granted	2004-07-27	2006-02-02	EASIC CORP
<input type="checkbox"/>	2	<a href="#">US20050117436A1</a>	Logic array devices having complex macro...	PGPub - Granted	2004-12-28	2005-06-02	COX WILLIAM D
<input type="checkbox"/>	3	<a href="#">US6823499B1</a>	Method for designing application specific i...	Lapsed	2002-09-16	2004-11-23	LSI CORP
<input type="checkbox"/>	4	<a href="#">US20060164121A1</a>	Structured integrated circuit device	PGPub - Granted	2006-03-03	2006-07-27	EASIC CORP
<input type="checkbox"/>	5	<a href="#">US20030144760A1</a>	Personalized hardware	PGPub - Granted	2002-12-16	2003-07-31	MANGELL EFRAIM
<input type="checkbox"/>	6	<a href="#">US20060028241A1</a>	Structured integrated circuit device	PGPub - Granted	2005-07-22	2006-02-09	EASIC CORP

Up to the 6th  
Degree List

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# Family Prior Art

# Family Prior Art of '625

Review prior art cited by and cited against the family counterparts when available

Simple Family

**1**

Backward Citation: Patent

**7**

Backward Citation: Non-Patent Literature

**0**

## Backward Citation: Patent

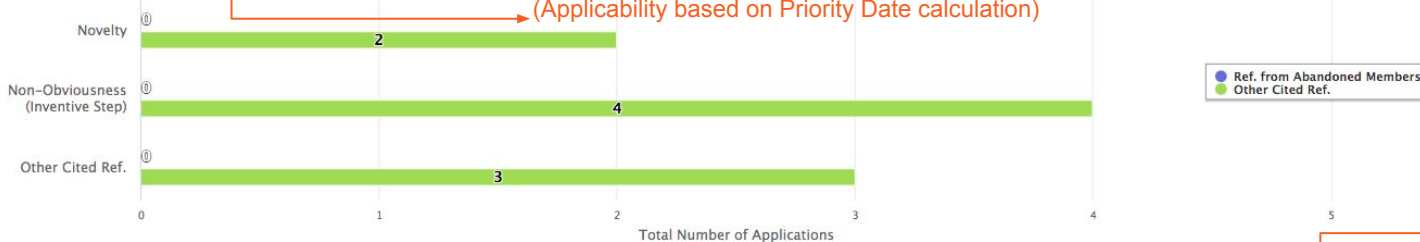
Categorized to indicate relevance; You can start from applicable references cited as novelty prior art

All References (7)

**Applicable Only (7)**

Choose Applicable Only

(Applicability based on Priority Date calculation)



Prior Art List

KEEP Mode

Ranked By : Appl. Date

<input type="checkbox"/>	#	Patent No.	Title	Legal Status	Appl. Date	Pub./Issue Date	Assignee (Std)	Applicability
<input type="checkbox"/>	1	<a href="#">US5452251A</a>	Semiconductor memory device for selectin...	Expired	1993-06-22	1995-09-19	FUJITSU LTD	(Pre-AIA) § 102(a) (Pre-AIA) § 102(b) (Pre-AIA) § 102(e)(2)
<input type="checkbox"/>	2	<a href="#">US5590072A</a>	Nonvolatile semiconductor memory device	Expired	1995-05-04	1996-12-31	SAMSUNG ELECTRONICS C...	(Pre-AIA) § 102(a) (Pre-AIA) § 102(b) (Pre-AIA) § 102(e)(2)
<input type="checkbox"/>	3	<a href="#">US5847420A</a>	Semiconductor integrated circuit having thr...	Expired	1997-01-28	1998-12-08	MITSUBISHI ELECTRIC CORP	(Pre-AIA) § 102(a) (Pre-AIA) § 102(b) (Pre-AIA) § 102(e)(2)

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# Semantic Prior Art

# Semantic Prior Art of '625

Review potential prior art ranked by concept similarity

## Semantic Prior Art

Most Relevant US, EP, JP, KR, CN & WO 300 prior art references based on **Semantic Similarity** among the first claims and abstracts

[Change Scope](#)

Select claim text or enter the desired text/keywords

Discover prior art's similarity with claim chart format in seconds !

KEEP Mode

0 are of high semantic similarity


Ranked By : Relevance

<input type="checkbox"/>		Ranking	Patent No.		Title	Legal Status	Appl. Date	Pub./Issue Date	Assignee (Std)	Applicability
<input type="checkbox"/>		1	<a href="#">JPH11-251466A</a>		FLASH MEMORY REGION FOR MEMORY DE...	Abandoned	1999-01-04	1999-09-17	TEXAS INSTRUMENTS INC	(Pre-AIA) § 102(a) (Pre-AIA) § 102(b)
<input type="checkbox"/>		2	<a href="#">US6472752B1</a>		Flash memory device	Expired	2000-11-22	2002-10-29	SK HYNIX INC	(Pre-AIA) § 102(e)(2)
<input type="checkbox"/>		3	<a href="#">US5682350A</a>		Flash memory with divided bitline	Abandoned	1996-10-07	1997-10-28	APLUS INTEGRATED CIRCU...	(Pre-AIA) § 102(a) (Pre-AIA) § 102(b) (Pre-AIA) § 102(e)(2)
<input type="checkbox"/>		4	<a href="#">WO1998/015959A1</a>		FLASH MEMORY WITH DIVIDED BITLINE	Abandoned	1997-10-03	1998-04-16	APLUS INTEGRATED CIRCU...	(Pre-AIA) § 102(a) (Pre-AIA) § 102(b)
<input type="checkbox"/>		5	<a href="#">US6339549B1</a>		Semiconductor storage apparatus having ...	Expired	2000-02-09	2002-01-15	NEC CORP	(Pre-AIA) § 102(e)(2)
<input type="checkbox"/>		6	<a href="#">EP0822598A1</a>		Single-chip contact-less read-only memory ...	Abandoned	1997-07-30	1998-02-04	NEC CORP	(Pre-AIA) § 102(a) (Pre-AIA) § 102(b)
<input type="checkbox"/>		7	<a href="#">US5777922A</a>		Flash memory device	Expired	1996-10-18	1998-07-07	HYUNDAI ELECTRONIC IND...	(Pre-AIA) § 102(a) (Pre-AIA) § 102(b) (Pre-AIA) § 102(e)(2)
<input type="checkbox"/>		8	<a href="#">WO1995/017010A1</a>		AN INCREASED-DENSITY FLASH EPROM T...	PCT End - NP	1994-12-15	1995-06-22	NATIONAL SEMICONDUCT...	(Pre-AIA) § 102(a) (Pre-AIA) § 102(b)

# Semantic Prior Art of '625

Review potential prior art ranked by concept similarity

Expired

**US6459625B1**


Three metal process for optimizing layout density

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[About Semantic Prior Art](#)

### Semantic Prior Art

Most Relevant US, EP, JP, KR, CN & WO 300 prior art references based on [Semantic Similarity](#) within the scope below. [Reset to Default](#)

+ Add text from claims

Submit

[Discover prior art's similarity with claim chart format in s](#)

Add text from claims


Select A Claim

1
2
3
4
5
6
7
8
9
10

Next 10

A method of electrically interconnecting a periphery area in a flash memory, comprising: providing a plurality of sub-circuits fabricated in a periphery area of a silicon substrate, wherein each sub-circuit includes at least one electrical circuit having a plurality of circuit components; partially electrically interconnecting said circuit components with a first metal interconnect layer including a plurality of first metal layer lines that are oriented substantially in one direction; completing the electrical interconnection of said circuit components in each respective sub-circuit with a second metal interconnect layer including a plurality of second metal layer lines that are

Add


adding text from claims to find more related Prior Art



---

# Comparison tools

# Prior Art Comparison (claim chart format)

What does this prior art say about the critical elements?

1.01

1.02

1.03

1.04

1.05

1.06

Find **24** Result(s) | Disclosure Rate : **66%**

### Claim Element

#1.01 A method of **electrically** interconnecting a **periphery area** in a **flash memory**, comprising:

**Keyword List** ⓘ

flash memory

(34)

FW

PA

electrically

(1)

FW

PA

periphery area

(0)

FW

### US6472752B1 Content

Abstract

A **flash memory** device is configured to address the problems that charges generated when via hole is etched is charged to a junction region through a metal line and are thus concentrated on a tunnel oxide film , thus making distribution of a threshold voltage over a cell uneven when a device is driven . In order to solve the problems , the device has a junction region in an outside circuit region so charges generated when via hole is etched is concentrated on the junction region formed in the outside circuit region . Thus , it can prevent concentration of the charges on the cell and thus make uniform distribution of the threshold voltage over a cell array .

Claims

**Claim# 1** A **flash memory** device , comprising : a **flash memory** cell formed in a cell array region of a substrate in which the cell array region and an outside circuit region are defined , the **flash memory** cell having a source region and a drain region in said cell array region ; a first junction region formed in said outside circuit region ; a first metal contact formed on said source region ; second and third metal contacts formed on said first junction region ; a first metal line connecting said first metal contact and said second metal contact ; a second metal line connected to said third metal contact ; and a via hole formed on said second metal line .

**Claim# 10** The **flash memory** device according to claim 9 , wherein the first junction region has a P junction structure if the **flash memory** cell is N - type , and has a N junction structure if the **flash memory** cell is P - type .

**Claim# 11** The **flash memory** device according to claim 9 , wherein the first junction region is surrounded by at least one well .

**Claim# 12** The **flash memory** device according to claim 9 , wherein the second metal line is present only in the outside circuit region .

**Answer the question:**

**What does this prior art say about the Claim elements: “flash memory” ?**

**Discover prior art similarity with keywords (includes keyword stemming) mapped to the selected prior art reference Abstract, Claims, and Specification.**

# Prior Art Comparison (sample output)

Easily generate a table like below

Claim		Claim-Term Interpretation	Semantic Prior Art - 752'	3rd Degree Citation Prior Art - B
1	A method of electrically interconnecting a periphery area in a flash memory, comprising:	Refer to Claim Analysis results	N/A	.....
	providing a plurality of sub-circuits fabricated in a periphery area of a silicon substrate, wherein	.....	N/A	.....
	each sub-circuit includes at least one electrical circuit having a plurality of circuit components;	.....	66%	
	partially electrically interconnecting said circuit components with a first metal interconnect layer including a plurality of first metal layer lines that are oriented substantially in one direction;	.....	80%	.....
	completing the electrical interconnection of said circuit components in each respective sub-circuit with a second metal interconnect layer including a plurality of second metal layer lines that are oriented substantially perpendicular to said first metal layer lines;	.....	60%	.....
	and electrically interconnecting each respective sub-circuit with a predetermined number of other sub-circuits with a third metal interconnect layer including a plurality of third metal layer lines.		N/A	

System-identified keywords and key phrases  
(highlighting of other keywords is available)

Results from claim to  
specification and file  
wrapper mapping

Results from prior art comparison by  
claim element

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# Prior art downloads

→ Select all



Download patent data in Excel or PDF format for Family Prior Art, Second Degree Prior Art, and/or Semantic Prior Art.

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# Prosecution and PTAB History

## Key Events

# Key Events - '625

1 Prosecution & 5 Post-Grant

Event History

**6**

Family Status

**1** Applications

Prior Art Status

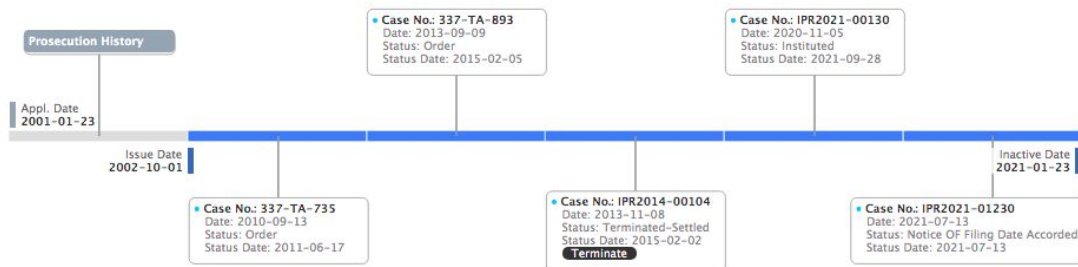
**380** Applications / **2** NPL References

Event History | **1** Prosecution History / **5** Post-Grant

Validity challenges to a patent in its prosecution history and post-grant events

# of Family Counterparts and Legal Status

# of Highly Relevant Prior Art References



Timeline of Prosecution:

☐ Other Document ☒ Rejection Document



# Key Events - '625

## Prosecution History

09/767341 Prior Art Ref. | 0 Ref.

Check prior art cited and the legal basis of these challenges

Double Patenting

0 Ref.

§ 102

0 Ref.

§ 103

0 Ref.

Summary of 09/767341 History | 1 Event(s)

Data Last Updated on: 2021-11-04

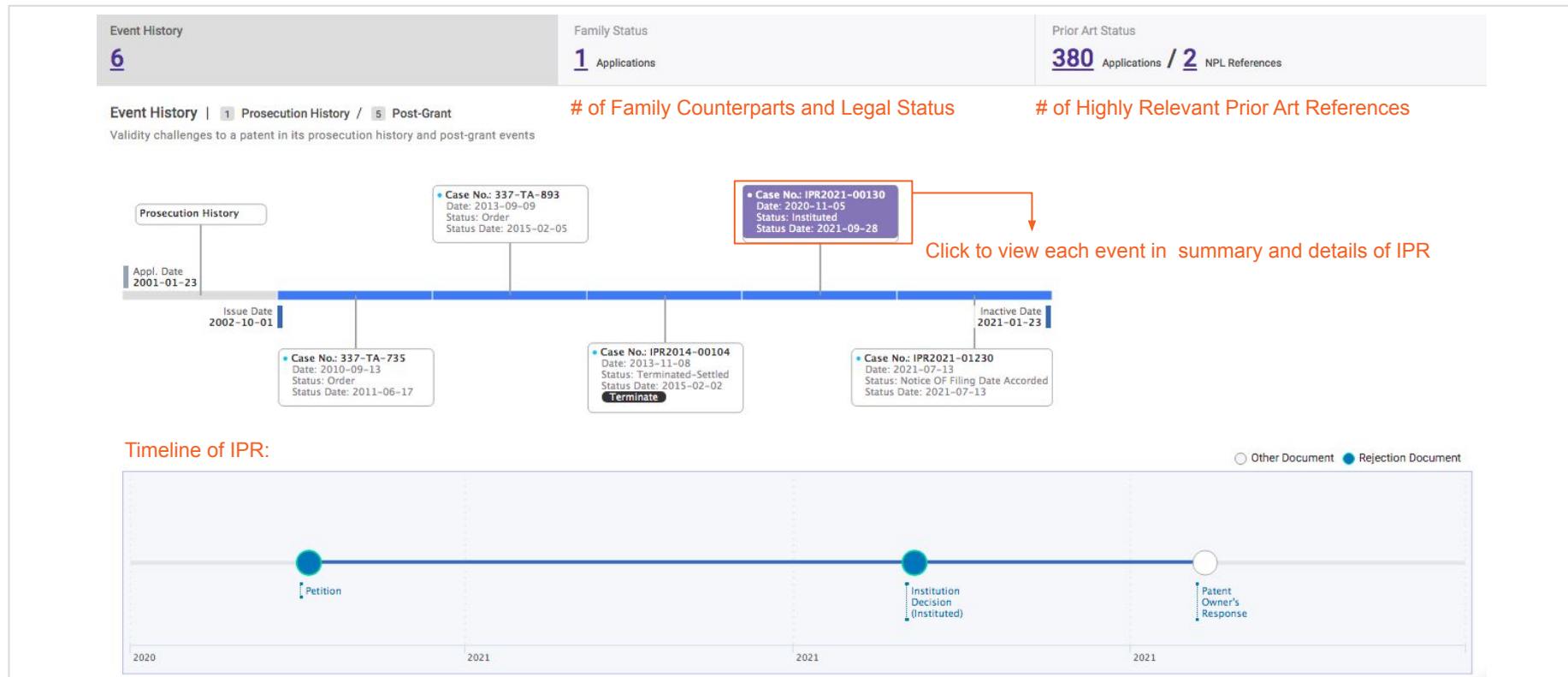
Descriptions (Code)	Date 	Prior Art Ref.
Claims (CLM)	2001-01-23	

Clickable events for original OAs and their OCR version when available.



# Key Events - '625

Post-Grant



# Key Events - '625

Post-Grant

IPR2021-00130 Prior Art Ref. | 4 Ref.

Check prior art cited and the legal basis of these challenges

Double Patenting

0 Ref.

§ 102

0 Ref.

§ 103

4 Ref.

[US6242767 \(1st\)](#)  
How

[other reference](#)  
CMOS Circuit Design

[US6433436](#)  
Feild

[US5452251](#)  
Akaogi

## Order

ORDERED that, pursuant to 35 U.S.C. § 314(a), an inter partes review of claims 1–12 and 14 of the '625 Patent is instituted with respect to all grounds set forth in the Petition; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and

Summary of IPR2021-00130 History | 3 Event(s)

Clickable events for original OAs and their OCR version when available.

Direct links to Grounds,

Claims Highlighted and Prior Art Details

Data Last Updated on: 2021-11-05

Descriptions (Code)	Date	Prior Art Ref.
Patent Owner's Response	2021-09-28	
Institution Decision (Instituted)	2021-06-14	Grounds 4
Legal Basis	Claims	Prior Art Ref.
35 U.S.C. § 103	claim 1,2,3,4,5,6,7,8,9,10,11,12,14	How <a href="#">US6242767 (1st)</a> Feild <a href="#">US6433436</a> CMOS Circuit Design (other reference)
35 U.S.C. § 103	claim 1,2,3,4,5,10,11,12,14	How <a href="#">US6242767 (1st)</a>
35 U.S.C. § 103	claim 6,7,8,9	How <a href="#">US6242767 (1st)</a> Feild <a href="#">US6433436</a>

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# Prosecution and PTAB History Search

# Patent File Wrapper Search

 Directly discover details in the prosecution history and post-grant proceeding across all documents via a keyword search.

## Cross-Document Search

Enter keyword to find documents including specific legal basis or specific claim terms

[① About File Wrapper Search](#)

touch sensor



## Rejections, Remarks, and Notice of Allowance in Prosecution History | 13 Records

<input type="checkbox"/> Descriptions (Code) 	Party	Date 
<input type="checkbox"/> Notice of Allowance (NOA)	USPTO	2015-09-24
<input type="checkbox"/> Applicant Arguments/Remarks Made in an Amendment (REM)	Applicant	2015-06-19
<input type="checkbox"/> Non-Final Rejection (CTNF)	USPTO	2015-03-19
<input type="checkbox"/> Request for Continued Examination (RCEX)	Applicant	2015-03-03
<input type="checkbox"/> Applicant Arguments/Remarks Made in an Amendment (REM)	Applicant	2015-03-03
<input type="checkbox"/> Final Rejection (CTFR)	USPTO	2014-11-03
<input type="checkbox"/> Applicant Arguments/Remarks Made in an Amendment (REM)	Applicant	2014-10-15
<input type="checkbox"/> Non-Final Rejection (CTNF)	USPTO	2014-07-15
<input type="checkbox"/> Request for Continued Examination (RCEX)	Applicant	2014-06-26
<input type="checkbox"/> Applicant Arguments/Remarks Made in an Amendment (REM)	Applicant	2014-06-26
<input type="checkbox"/> Final Rejection (CTFR)	USPTO	2014-02-26
<input type="checkbox"/> Applicant Arguments/Remarks Made in an Amendment (REM)	Applicant	2014-02-07
<input type="checkbox"/> Non-Final Rejection (CTNF)	USPTO	2013-11-07

Data Last Updated on 2021-04-08

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# Prosecution and PTAB History PDF Downloads

# PDF Downloads

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### Cross-Document Search

Enter keyword to find documents including specific legal basis or specific claim terms

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Rejections, Remarks, and Notice of Allowance in Prosecution History | 13 Records

<input type="checkbox"/> Descriptions (Code)	Party	Date
<input type="checkbox"/> Notice of Allowance (NOA)	USPTO	2015-09-24
<input type="checkbox"/> Applicant Arguments/Remarks Made in an Amendment (REM)	Applicant	2015-06-19
<input type="checkbox"/> Non-Final Rejection (CTNF)	USPTO	2015-03-19
<input type="checkbox"/> Request for Continued Examination (RCEX)	Applicant	2015-03-03
<input type="checkbox"/> Applicant Arguments/Remarks Made in an Amendment (REM)	Applicant	2015-03-03
<input type="checkbox"/> Final Rejection (CTFR)	USPTO	2014-11-03
<input type="checkbox"/> Applicant Arguments/Remarks Made in an Amendment (REM)	Applicant	2014-10-15
<input type="checkbox"/> Non-Final Rejection (CTNF)	USPTO	2014-07-15
<input type="checkbox"/> Request for Continued Examination (RCEX)	Applicant	2014-06-26
<input type="checkbox"/> Applicant Arguments/Remarks Made in an Amendment (REM)	Applicant	2014-06-26
<input type="checkbox"/> Final Rejection (CTFR)	USPTO	2014-02-26
<input type="checkbox"/> Applicant Arguments/Remarks Made in an Amendment (REM)	Applicant	2014-02-07
<input type="checkbox"/> Non-Final Rejection (CTNF)	USPTO	2013-11-07

Data Last Updated on 2021-04-08

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# Prosecution and PTAB History Side-by-side PDF and OCR

# Side by Side: PDF & OCR



Conduct a keyword search in a single document to identify the claim scope quickly and easily. You can even search additional claim terms within rejections.

**Keywords (2)**

Select a Keyword Set

☐ sensor (23)

☐ flexible substrate (1)

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U9926631182 - CTNF (2015-03-19)

13/284,674 6 / 18 90%

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Art Unit: 2867

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the touch panel taught by Grant by adding drive or sense electrodes made of flexible conductive material as taught by Hotelling since the sensor traces provide level shifting from a low voltage level to a higher voltage level, thus providing a better signal-to-noise ratio for improved noise reduction purposes while the drive traces provide shielding for the sense traces.

Neither Grant nor Hotelling specifically teach wherein the flexible conductive material of the drive or sense electrodes comprises first and second conductive lines that electrically contact one another at an intersection.

However, Gray does teach wherein the flexible conductive material of the drive or sense electrodes comprises first and second conductive lines that electrically contact one another at an intersection (Fig. 2; [0063]: **A number of conductors forming rows and columns of a conductive pattern (e.g., indium tin oxide (ITO)) may be deposited on a substrate composed of polyester or other material on one or more layers of the touchscreen... the row and column oriented conductors may be disposed on the same layer...**; See also Miller US 5,089,672; Col. 2, lines 11-16; Col. 5, lines 1-20; Col. 5, lines 61-68).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the combination of Grant and Hotelling by including the conductive lines (rows and columns) taught by Gray for the purpose of "providing paths for signals traveling through the touchscreen" (See Gray; Abstract).

103(a) as being unpatentable over Grant et al. US 2008/0303782 A1 (previously cited and  
... PAGE 5 ...

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hereinafter Grant) in View of Hotelling et al. US 2008/0158183 A1 (previously cited and hereinafter Hotelling), in further View of Gray et al. US 2010/0045614 (previously cited and hereinafter Gray) and in further View of Frey et al. US 2009/0219257 (newly cited and hereinafter Frey).

Regarding claim 1, Grant does teach an apparatus (Abstract) comprising:  
a substantially flexible substrate (Abstract: flexible touch sensitive surface); and  
a touch [0003], [0005], [0006], [0022], [0023], [0027], and [0071], e.g., flexible surface, flexible circuitry, and capacitance touch [0003] which must be conductive to receive user input) disposed on the substantially flexible substrate ( see at least Figs. 1A-1C; [0009-0011], configured to bend with the substantially flexible substrate (Figs. 1A-1C, 3 and the corresponding descriptions; [0003]).

Grant does not specifically teach the touch [0003] comprising drive or sense electrodes made of flexible conductive material.

However, Hotelling does teach a touch [0003] (Fig. 2a, 5 and the corresponding descriptions, and the Summary of the Invention, i.e., a touch [0003] comprises of row and column traces made of copper) comprising drive or sense electrodes (see at least Figs. 1 and 2a; [0008, 0030-0033]; claim 9; sense traces formed on a first side of a dielectric substrate; and drive traces formed on a second side of the substrate) made of flexible conductive material ([0008]; traces made of copper or other highly conductive metals running along the edge of the substrate).

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It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the touch panel taught by Grant by adding drive or sense electrodes made of flexible conductive material as taught by Hotelling since the [0003] traces provide level shifting from a low voltage level to a higher voltage level, thus providing a better signal-to-noise ratio for improved noise reduction purposes while the drive traces provide shielding for the sense traces.

Neither Grant nor Hotelling specifically teach wherein the flexible conductive material of the drive or sense electrodes comprises first and second conductive lines that electrically contact one another at an intersection.





## QI is a Game Changer

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